Docket No.: GS150

CLAIMS:

1. A trench MOSFET transistor device comprising:

a silicon substrate of a first conductivity type;

a silicon epitaxial layer of said first conductivity type over said substrate, said epitaxial layer having a lower majority carrier concentration than said substrate;

a trench extending into said epitaxial layer from an upper surface of said epitaxial layer;

an insulating layer lining at least a portion of said trench;

a conductive region within said trench adjacent said insulating layer;

a body region of a second conductivity type provided within an upper portion of said epitaxial layer and adjacent said trench;

a source region of said first conductivity type provided within an upper portion of said body region and adjacent said trench;

an upper region of second conductivity type within an upper portion of said body region and adjacent said source region, said upper region having a higher majority carrier concentration than said body region; and

a source contact region disposed on said epitaxial layer upper surface, said source contact region comprising: (a) a doped polycrystalline silicon contact region in electrical contact with said source region and (b) a metal contact region adjacent said doped polycrystalline silicon contact region and in electrical contact with said source region and with said upper region.

2. The trench MOSFET transistor device of claim 1, wherein said metal contact region comprises aluminum.

3. The trench MOSFET transistor device of claim 1, wherein said doped polycrystalline silicon contact region is an N-type polycrystalline silicon region.

4. The trench MOSFET transistor device of claim 3, wherein said doped polycrystalline silicon contact region has a doping concentration ranging from $5x10^{19}$ to $1x10^{20}$ cm^{-3}.

5. The trench MOSFET transistor device of claim 1, wherein said doped polycrystalline silicon contact region is substantially triangular in cross-section.

6. The trench MOSFET transistor device of claim 1, further comprising an insulating region disposed over said conductive region, said insulating region extending above said epitaxial layer upper surface.

7. The trench MOSFET transistor device of claim 6, wherein insulating region is a borophosphosilicate glass region.

8. The trench MOSFET transistor device of claim 6, wherein said doped polycrystalline silicon contact region is positioned laterally adjacent to said insulating region.

9. The trench MOSFET transistor device of claim 8, wherein a thickness of said doped polycrystalline silicon contact region is greatest adjacent said insulating region, and wherein an upper surface of said doped polycrystalline silicon contact region slopes away from said insulating region.

10. The trench MOSFET transistor device of claim 1, further comprising an additional region of second conductivity type immediately below said upper region, said additional region having a higher majority carrier concentration than said body region.

11. The trench MOSFET transistor device of claim 1, wherein said device comprises a plurality of transistor cells of square geometry or hexagonal geometry.

12. The trench MOSFET transistor device of claim 1, wherein said insulating layer is a silicon oxide layer.

13. The trench MOSFET transistor device of claim 1, wherein the conductive region comprises doped polycrystalline silicon.

14. The trench MOSFET transistor device of claim 1, wherein said first conductivity type

is N-type conductivity and said second conductivity type is P-type conductivity.

15. The trench MOSFET transistor device of claim 1, wherein said substrate is an N+ substrate, said epitaxial layer is an N epitaxial layer, said body region is a P region, said source region is an N+ region, and said upper region is a P+ region.

16. A trench MOSFET transistor device comprising:

an N-type silicon substrate;

an N-type silicon epitaxial layer over said substrate, said epitaxial layer having a lower majority carrier concentration than said substrate;

a trench extending into said epitaxial layer from an upper surface of said epitaxial layer;

a silicon oxide insulating layer lining at least a portion of said trench;

a doped polycrystalline silicon conductive region within said trench adjacent said insulating layer;

a P-type body region provided within an upper portion of said epitaxial layer and adjacent said trench;

an N-type source region provided within an upper portion of said body region and adjacent said trench;

a P-type upper region within an upper portion of said body region and adjacent said source region, said upper region having a higher majority carrier concentration than said body region;

a borophosphosilicate glass insulating region disposed over said conductive region, said insulating region extending above said epitaxial layer upper surface; and

a source contact region disposed on said epitaxial layer upper surface and laterally adjacent said insulating region, said source contact region comprising: (a) a doped polycrystalline silicon contact region having N-type doping and (b) a metal contact region adjacent said doped polycrystalline silicon contact region and in electrical contact with said source region and with said upper region.

17. A method of forming a trench MOSFET transistor device comprising:

providing a silicon substrate of a first conductivity type;

depositing a silicon epitaxial layer of said first conductivity type over said substrate, said epitaxial layer having a lower majority carrier concentration than said substrate;

etching a trench extending into said epitaxial layer from an upper surface of said epitaxial layer;

forming an insulating layer that lines at least a portion of said trench;

forming a conductive region within said trench and adjacent said insulating layer;

forming a body region of a second conductivity type within an upper portion of said epitaxial layer and adjacent said trench;

forming a source region of said first conductivity type within an upper portion of said body region and adjacent said trench;

forming an upper region of second conductivity type within an upper portion of said body region and adjacent said source region, said upper region having a higher majority carrier concentration than said body region; and

forming a source contact region on said epitaxial layer upper surface, said source contact region comprising (a) a doped polycrystalline silicon contact region in electrical contact with said source region and (b) a metal contact region adjacent said doped polycrystalline silicon contact region and in electrical contact with said source region and with said upper region.

18. The method of claim 17, further comprising forming an insulating region over said conductive region, said insulating region extending above said epitaxial layer upper surface.

19. The method of claim 18, wherein insulating region is a borophosphosilicate glass region.

20. The method of claim 18, wherein said source contact region is formed by a process comprising: (a) providing a layer of doped polycrystalline silicon over said insulating region and said epitaxial layer upper surface; (b) etching said layer of doped polycrystalline silicon until a portion of said epitaxial layer upper surface is exposed and a portion of said doped polycrystalline silicon remains adjacent said insulating region,

and (c) depositing a metal layer over said insulating region, said epitaxial layer upper surface, and said remaining portion of said doped polycrystalline silicon adjacent said insulating region.

21. The method of claim 20, wherein said layer of doped polycrystalline silicon layer is etched by reactive ion etching.